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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,462	05/11/2005	Daniel Chatroux	123886	5027

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EXAMINER	
MEMULA, SURESH	
ART UNIT	**PAPER NUMBER**
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,462	CHATROUX ET AL.	
	Examiner	Art Unit	
	Suresh Memula	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 5/4/07
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to the amendments and remarks filed on 07/27/2007. The remarks are not persuasive; therefore, the rejections based on the prior art of record, Myono et al., are maintained. Claims 16-30 are pending.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "same clock signal is applied to the clock input of all subassemblies, **directly** (emphasis added)" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claim 16 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement**. The claim contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added limitation "same clock signal is applied to the clock input of all subassemblies, **directly** (emphasis added)" is not disclosed in the specification in full, clear, concise, and exact terms.

5. Furthermore, the response filed on 07/27/2007 fails to identify where in the specification support/clarification for the newly added limitations can be found.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 16-28 are rejected under 35 U.S.C. 102(e)** as being anticipated by US Patent No. 6,946,899 to Myono (Myono).

8. As to Claim 16,

an integrated circuit (FIG. 1, 6, 9-10, 12-13) comprising at least a digital part (FIG. 1, 2C, 3C, 4-5, 7-8) comprising a plurality transistors connected to one another so as to form a plurality of functional elements (FIG. 1, 6, 9-10, 12-13),

the functional elements being grouped in subassemblies (FIG. 1, 6, 9-10, 12-13) each comprising a first and a second electrical supply terminal (FIG. 1, 6, 9-10, 12-13) and a clock input (FIG. 1, 6, 9-10, 12-13),

the subassemblies being connected in series by means of their supply terminals to the terminals of a voltage supply source (Column 5, line 4; FIG. 1, 6, 9-10, 12-13),

wherein a same clock signal is applied to the clock input of all subassemblies, directly or by means of a device for shifting the levels of the clock signals (Column 5, lines 19-21; Column 6, lines 9-11; FIG. 1, 4, 6, 9-10, 12-13).

9. As to Claim 17, wherein the subassemblies are formed in such a way that the same current flows through the different subassemblies (Column 5, line 4; FIG. 1, 6, 9-10, 12-13; Myono teaches a series connection, e.g., all elements in a series connection have equal currents).

10. As to Claim 18, wherein the clock inputs of at least two adjacent subassemblies are connected by a device for shifting the clock signal levels (FIG. 1, 6, 9-10, 12-13).

11. As to Claim 19, wherein the clock input of one of the end subassemblies is connected by means of an additional device for shifting the clock signal levels at the output of the clock circuit (FIG. 1, 6, 9-10, 12-13).

12. As to Claim 20, wherein the device for shifting the clock signal levels comprises at least one capacitor (FIG. 1, 6, 9-10, 12-13).

13. As to Claim 21, wherein the device for shifting the clock signal levels comprises at least one transistor (FIG. 1, 6, 9-10, 12-13).

14. As to Claim 22, wherein all the subassemblies are identical (Column 6, lines 48-67; Column 7, lines 1-11; Column 9, lines 56-60; FIG. 1, 6, 9-10, 12-13).

15. As to Claim 23, wherein each of the subassemblies comprises a voltage limiting circuit connected between its power supply terminals (Column 2, lines 23-33; FIG. 1, 6, 9-13).

16. As to Claim 24, wherein the voltage limiting circuit comprises a diode (Column 2, lines 23-33; FIG. 1, 6, 9-13).

17. As to Claim 25, wherein the voltage limiting circuit comprises a transistor (Column 2, lines 23-33; FIG. 1, 6, 9-13).

18. As to Claim 26, wherein each subassembly comprises a decoupling capacitor connected between the first power supply terminal and the second power supply terminal of the subassembly (FIG. 1, 6, 9-10, 12-13).

19. As to Claim 27, wherein the integrated circuit comprises means for electrical insulation between the subassemblies (FIG. 1, 6, 9-13).

20. As to Claim 28, wherein the means for electrical insulation between the different subassemblies are reverse biased diode junctions (Column 2, lines 23-33; FIG. 1, 6, 9-13).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. **Claim 29 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Myono in view of US Pub. No. 2002/0014663 to Iwamatsu et al. (Iwamatsu).

23. Myono substantially teaches all of the limitations as stated above, except for dielectric zones.

24. Iwamatsu discloses dielectric zones (Paragraph 0002).

25. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have utilized dielectric zones; as taught by Iwamatsu (Paragraph 0002); in order to obtain higher performance by isolating circuit elements.

26. **Claim 30 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Myono in view of one or more of:

US Pub. No. 2004/0077151 to Bhattacharyya (Bhattacharyya),

US Pub. No. 2004/0087084 to Hsieh (Hsieh),

US Pub. No. 2004/0094763 to Agnello et al. (Agnello), and/or

US Pub. No. 2004/0018668 to Maszara (Maszara).

27. Myono substantially teaches all of the limitations as stated above, except for silicon-on-insulator.

28. Bhattacharyya discloses silicon-on-insulator (Abstract; Paragraphs 0004, 0015), Hsieh discloses silicon-on-insulator (Paragraph 0024), Agnello discloses silicon-on-insulator (Paragraph 0049), and Maszara discloses silicon-on-insulator (Paragraph 0002).

29. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have utilized silicon-on-insulator; as taught by Bhattacharyya (Abstract; Paragraphs 0004, 0015), Hsieh (Paragraph 0024), Agnello (Paragraph 0049), and/or Maszara (Paragraph 0002); in order to provide advantages of significant speed, power, and radiation immunity (Bhattacharyya: Paragraph 0004), reduce undesired capacitance (Maszara: Paragraph 0002), suppress short channel effect (Maszara: Paragraph 0002), and/or reduce latch-up and soft errors (Maszara: Paragraph 0002); since silicon-on-insulators are well-documented (Maszara: Paragraph 0002), well-known in the art (Hsieh: Paragraph 0024) and conventional (Bhattacharyya: Abstract; Paragraph 0015; Agnello: Paragraph 0049).

Response to Applicant Remarks

30. The applicant states Myono teaches two subassemblies driven by four clock signals and fails to teach the amended limitation of "wherein a same clock signal is applied to the clock input of all subassemblies".

Examiner's response:

31. The applicant's amendment broadly requires a same clock signal applied to all subassemblies, but the amended claim language does not prohibit either a plurality of clock signals in addition to the same clock signal or prohibit a same clock signal with different signal levels.

32. Accordingly, the teachings of Myono are interpreted to anticipate amended claim 16 for one or more of the following reasons:

(i) a clock driver originates a "same clock signal" that is the basis for clock pulses CLK, CLKB, CLK' and CLKB' of different signal levels (Myono: Column 5, lines 19-21; Column 6, lines 9-11; FIG. 4); and/or

(ii) Myono teaches a first subassembly (FIG. 1, elements #M3, M4, S3, S4) receives clock signal CLK (FIG. 1), and a second subassembly (FIG. 1, elements #M1, M2, S1, S2) receives the same clock signal CLK (FIG. 1).

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suresh Memula
Art Unit 2825
October 10, 2007

PAUL DINH
PRIMARY EXAMINER

Paul Dinh